RF AND MECHANICAL CHARACTERIZATION OF FLIP-CHIP INTERCONNECTS IN CPW CIRCUITS WITH UNDERFILL

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Abstract **RF characterization of flip-chip interconnects in CPW circuits with underfill has been investigated by measuring the scattering-parameters up to 40 GHz for GaAs coplanar waveguide (CPW) through line chips flip-chip mounted on alumina substrate with and without underfill epoxy. Fatigue life of flip-chip assemblies has been computed for different chip sizes and substrates. The results show feasibility of using underfill encapsulant in microwave/mm-wave frequency range.**

I. Introduction

Because of several advantages compared to wire bonding (low cost, better performance, high reliability, etc.), RF and microwave assembly packages are increasingly likely to use flip-chip bonding instead of wire bonding [1]. Generally, flip-chip assembly requires underfill to reduce the stress on joints during thermal excursions, to increase the fatigue life of joints, and to protect the assembly from environment [2 - 7]. However, the underfill material affects the electrical performance of the assembly due to its different dielectric constant and dissipation factor (tanδ) compared to those of air. The only study so far reported the effect of Sealgard (ε_r =2.8) and Globtop (ε_r =3.14) on performance of an LNA in the frequency range from 5 to 15 GHz [8]. In this paper, both electrical and mechanical characterization of CPW flip-chip assembly with underfill encapsulant are reported. The effects of underfill encapsulant on RF performance are characterized up to 40 GHz based on measurements on CPW flip-chip assemblies. Fatigue life of flip-chip assemblies is studied by finite element method (FEM).

II. Test circuits and assembly

Two GaAs chips containing CPW sections were selected for experiment [9]. Chip #1, with dimensions of 1.106mm x 1.380mm x 0.635mm, has a 50Ω CPW through line of length 0.600mm fabricated on it. Chip #2, with length of 4.700mm, is longer than chip #1 and has a 4.125 mm through CPW line on it. On these test chips, six silver bumps were plated on the ends of CPW line and the edges of ground planes. The dimension of the bumps is 75um in height and 150um in diameter. Multi-line-TRL calibration set and the circuits for mounting GaAs chips were designed using 50Ω CPW transmission lines and fabricated on a single 25.4mm x 25.4mm alumina substrate. Layout dimensions were modified to compensate for the effect of overetching [10]. Figure 1 shows the layout of a circuit fabricated on the alumina substrate.

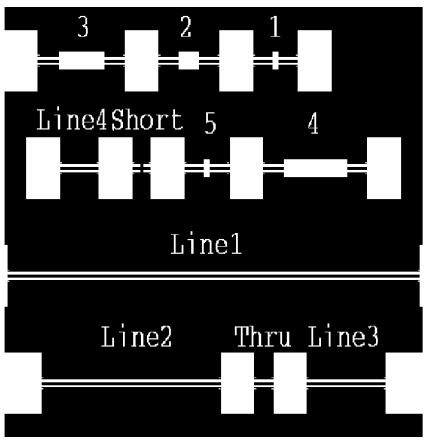

Figure 1. Layout of calibration standard set and carrier circuits on alumina substrate.

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The GaAs chips were mounted on the alumina substrate by thermosonic flip-chip bonding [11]. The parameters selected for this operation were: temperature 180°C, bonding force 1.575kg, and ultrasonic power 8.5W. After bonding, the epoxy (U300 from Epoxy Tech. Inc., with ε_r=4.1 and tanδ=0.009 at 100 KHz) was underfilled in gaps between chips and the substrate and cured at 120 °C for 25 minutes.

RF measurements were performed on a HP8510 network analyzer with on-wafer probes for a frequency range extending to 40 GHz. Measurements on assemblies for chip #1 and chip #2 were carried out before as well as after adding the underfill encapsulant.

III. RF measurement results and characterization

Figures 2 and 3 show measured S-parameters of the flip-chip assembly for chip #1 with and without underfill as a function of frequency, and Figures 4 and 5 show the same for the assembly with chip #2. Comparing the measured results of the two flip-chip assemblies with and without underfill, we see two kinds of effects due to underfill: the return loss and insertion loss of flip-chip assemblies increase, and the frequencies of minimum reflection shift downwards.

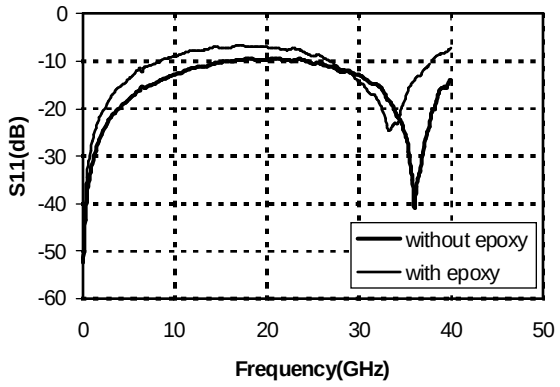

Figure 2. Comparison of measured S_{11} of flip-chip assembly with and without underfill for chip #1.

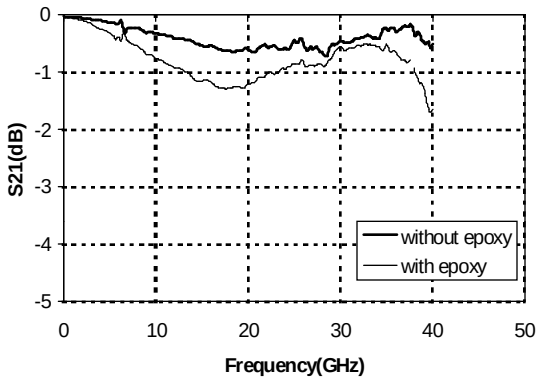

Figure 3. Comparison of measured S_{21} of flip-chip assembly with and without underfill for chip #1.

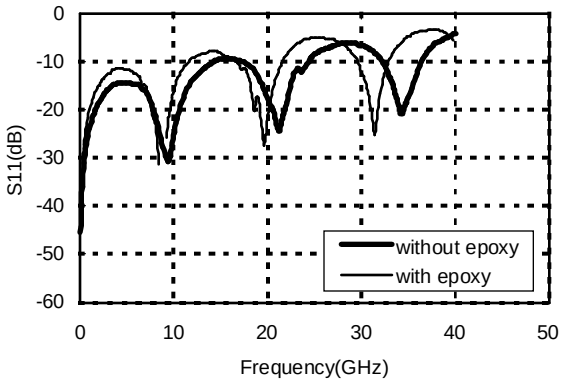

Figure 4. Comparison of measured S_{11} of flip-chip assembly with and without underfill for chip #2.

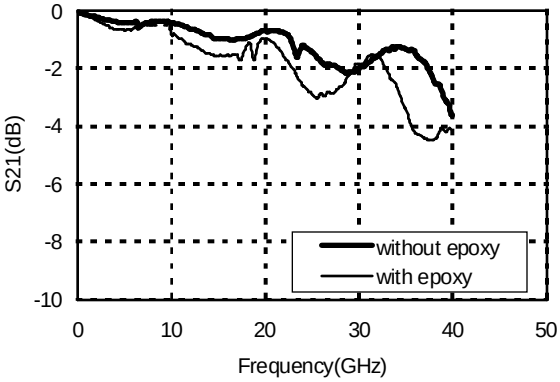

Figure 5. Comparison of measured S_{21} of flip-chip assembly with and without underfill for chip #2.

A. Losses

The loss in the flip-chip assembly includes the loss of the CPW on the alumina substrate and the loss of the CPW on GaAs. After addition of underfill, the presence of epoxy increases the loss. Figures 6 and 7 show the loss of the flip-chip assemblies with and without underfill epoxy for chip #1 and chip #2, respectively, as a function of frequency. The additional loss due to underfill epoxy is small. In fact, the additional loss is less than 0.6 dB for the flip-chip assembly with chip #1 and less than 1 dB for the flip-chip assembly with chip #2 at 40 GHz.

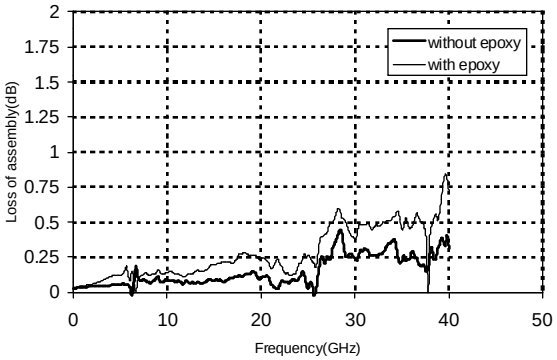

Figure 6. Comparison of loss of flip-chip assembly with and without underfill epoxy for chip #1.

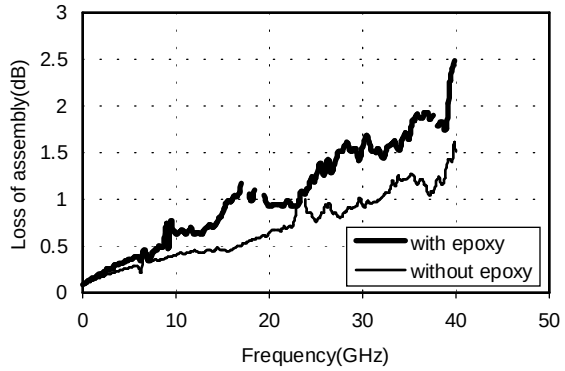

Figure 7. Comparison of loss of flip-chip assembly with and without underfill epoxy for chip #2.

B. Change in ε_{re} of CPW on GaAs

The shift in frequencies of minimum reflection can be attributed to the difference in the values of effective dielectric constant of CPW with and without underfill epoxy. Effective dielectric constants of CPW on GaAs with and without underfill (as computed by EM simulation on HP-HFSS) are 7.259 and 8.917, respectively. The difference is about 23 percent. Table I shows the measured and calculated (using the computed values of the effective dielectric constants) frequencies of minimum reflection for the two assemblies. The good agreement between the measured and calculated frequencies for minimum reflection validates the accuracy of our measurements and modeling.

Chip number	Meas. freq. for min. reflection w/o epoxy (GHz)	Meas. freq. for min. reflection with epoxy (GHz)	Cal. freq. for min. reflection with epoxy (GHz)
Chip#1	36.0050	32.2085	32.4857
Chip#2	34.2073	31.4108	30.8637
Chip#2	21.2235	19.6255	19.1490
Chip#2	9.4383	8.4385	8.5157

Table I. Comparison of measured and calculated frequencies for minimum reflection.

IV. Mechanical Characterization of flip chip assembly with underfill encapsulant

Thermomechanical stresses on the joints because of coefficient of thermal expansion (CTE) mismatch between the flipped chip and the substrate result in thermomechanical fatigue and consequent failure of the assembly. This stress can be reduced by encapsulation of the joint with an underfill encapsulating material, which enhances the reliability of the assembly. Underfill encapsulant has been widely employed to enhance the reliability of bonding joints in lower-frequency and digital electronic assemblies.

FEM simulation was used to analyze fatigue life of the flip-chip assembly. The mechanical properties of materials used for FEM simulation are listed in Table II. Inelastic strain energy density is computed using FEM to calculate fatigue life of flip-chip joints for different chip sizes and substrates[12]. Figure 8 shows results for fatigue life with and without underfill encapsulant for GaAs chips on alumina and duroid. The results indicate that without underfill the larger chip has a shorter fatigue life, and with underfill all assemblies have better fatigue life. In fact, for chip #1 (L=0.600mm) mounted on the alumina substrate, the fatigue life increases from

5000 to 14000 cycles after the addition of underfill epoxy.

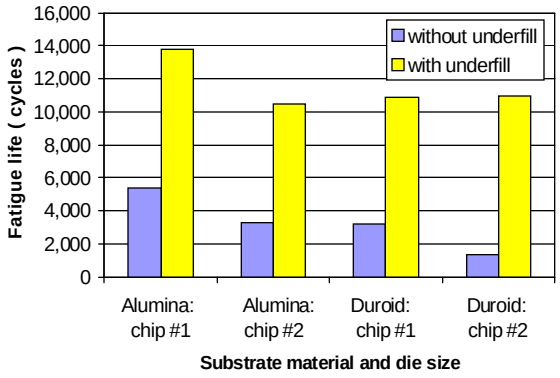

Figure 8. FEM results for fatigue life analysis of flip-chip assembly joints.

	CTE ($x10^{-6}$/°C)	Modulus (Mpa)	Temp. of glass transition (°C)
GaAs	5.7	112815	
U300 (Epoxy)	105	7500	130
Duroid	17	2070	
Alumina	5.6	372384	

Table II. The material properties used in FEM simulation for thermomechanical fatigue.

V. Concluding Remarks

The investigations reported in this paper show that the U300 epoxy (from Epoxy Tech. Inc.) with ε_r=4.1, tanδ=0.009 (measured at 100 kHz) can be used for flip-chip assemblies up to 40 GHz with only a small additional loss. The effect of the change in ε_{re} can be compensated by modifying the line lengths appropriately. By choosing an underfill epoxy with lower loss and lower dielectric constant, the effects of underfill could be reduced further

Acknowledgments

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References

[1] T. Goodman and E. Vardaman, "The flip chip market," Advanced Packaging, September/October 1997, pp. 24-26.

[2] W. Zhang, et al., "The effect of underfill epoxy on mechanical behavior of flip chip assembly," 1997 Proceedings. 47th Electronic Components and Technology Conference, pp. 1294, 1170-5.

[3] Y. Ohshima, et al., "Flip chip underfill reliability of CSP during IR reflow soldering," 1997 IEEE International Reliability Physics Symposium Proceedings, 35th Annual, pp. 124-128.

[4] D. Zoba and M. Edwards, "Review of underfill encapsulant development and performance of flip chip applications," 1996 Proceedings of the SPIE - The International Society for Optical Engineering, Vol. 2649, pp. 354-358.

[5] B. Wun and J. Lau, "Characterization and evaluation of the underfill encapsulants for flip chip assembly," Circuit World, Vol. 21, No. 3, pp. 25-27.

[6] C. Beddingfield and L. Higgins, "Alternative underfill methods for flip chip applications," SMTA National Symposium Emerging Packaging Technologies' Proceedings of The Technical Program, 1997, pp. 138, 21-7.

[7] R. Lachance, et al., "Corrosion/migration study of flip chip underfill and ceramic overcoating," 1997 Proceedings. 47th Electronic Components and Technology Conference, pp. 1294, 885-889.

[8] R. Sturdivant, et al., "Investigation of MMIC flip chips with Sealant for improved reliability without hermeticity," 1996 IEEE MTT-S Digest, pp. 239-242.

[9] Obtained from Hughes Aircraft Co.

[10] R. Marks, "A multiline method of network analyzer calibration," IEEE Transactions on Microwave Theory and Techniques, Vol. 39, July 1991, pp. 1205-1215.

[11] T. McLaren, et al., "Thermosonic bonding for flip chip assembly," Advancing Microelectronics, July/August 1994. pp. 14-16.

[12]. J. H. Lau, "Ball Grid array Technology," McGraw-Hill, 1995